

LE25S40QE



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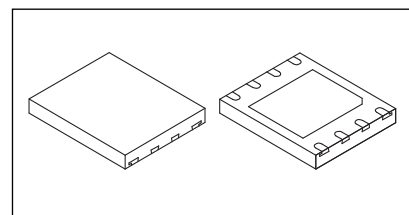
Advance Information

CMOS LSI

4M-bit (512K x 8) Serial Flash Memory

Overview

The LE25S40QE is a SPI bus flash memory device with a 4M bit (512K × 8-bit) configuration. It uses a single 1.8V power supply. While making the most of the features inherent to a serial flash memory device, the LE25S40QE is housed in an 8-pin ultra-miniature package. All these features make this device ideally suited to storing program in applications such as portable information devices, which are required to have increasingly more compact dimensions. The LE25S40QE also has a small sector erase capability which makes the device ideal for storing parameters or data that have fewer rewrite cycles and conventional EEPROMs cannot handle due to insufficient capacity.



VDFN8 5x6, 1.27P / VSON8T (6x5)

Features

- Read/write operations enabled by single 1.8V power supply: 1.65 to 1.95V supply voltage range
- Operating frequency : 40MHz
- Temperature range : -40 to 85°C
- Serial interface : SPI mode 0, mode 3 supported
- Sector size : 4K bytes/small sector, 64K bytes/sector
- Small sector erase, sector erase, chip erase functions
- Page program function (256 bytes / page)
- Block protect function
- Highly reliable read/write
 - Number of rewrite times : 100,000 times
 - Small sector erase time : 40ms (typ), 150ms (max)
 - Sector erase time : 80ms (typ), 250ms (max)
 - Chip erase time : 300ms (typ), 3.0s (max)
 - Page program time : 6.0ms/256 bytes (typ), 8.0ms/256 bytes (max)
- Status functions : Ready/busy information, protect information
- Data retention period : 20 years
- Package : VDFN8 5x6

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 22 of this data sheet.

Figure 2 Block Diagram

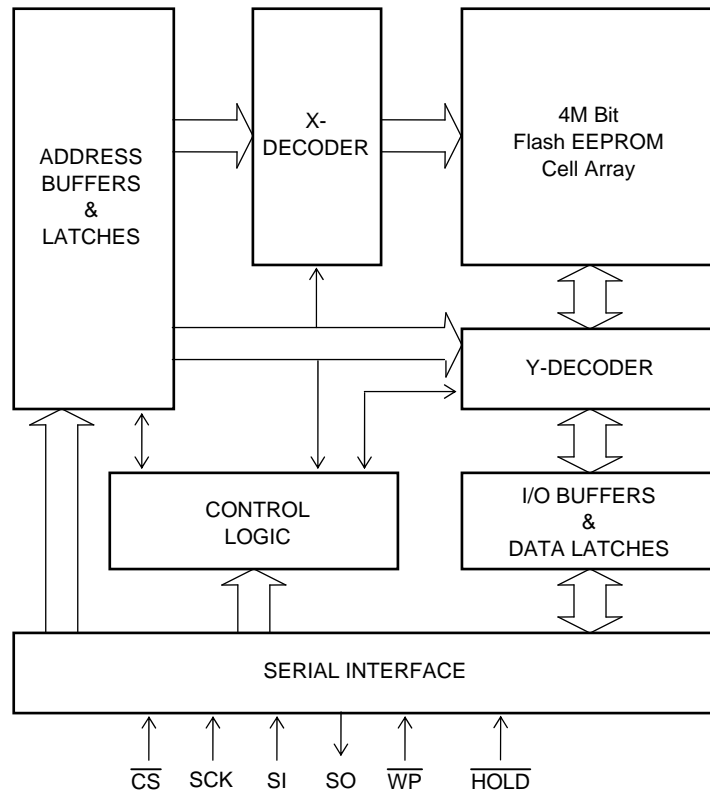


Table 1 Pin Description

Symbol	Pin Name	Description
SCK	Serial clock	This pin controls the data input/output timing. The input data and addresses are latched synchronized to the rising edge of the serial clock, and the data is output synchronized to the falling edge of the serial clock.
SI	Serial data input	The data and addresses are input from this pin, and latched internally synchronized to the rising edge of the serial clock.
SO	Serial data output	The data stored inside the device is output from this pin synchronized to the falling edge of the serial clock.
$\overline{\text{CS}}$	Chip select	The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high.
$\overline{\text{WP}}$	Write protect	The status register write protect (SRWP) takes effect when the logic level of this pin is low.
$\overline{\text{HOLD}}$	Hold	Serial communication is suspended when the logic level of this pin is low.
V_{DD}	Power supply	This pin supplies the 1.65 to 1.95V supply voltage.
V_{SS}	Ground	This pin supplies the 0V supply voltage.

Device Operation

The read, erase, program and other required functions of the device are executed through the command registers. The serial I/O corrugate is shown in Figure 3 and the command list is shown in Table 2. At the falling \overline{CS} edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are normalized in 8 bit units and taken into the device interior in synchronization with the rising edge of SCK, which causes the device to execute operation according to the command that is input.

The LE25S40QE supports both serial interface SPI mode 0 and SPI mode 3. At the falling \overline{CS} edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

Figure 3 I/O waveforms

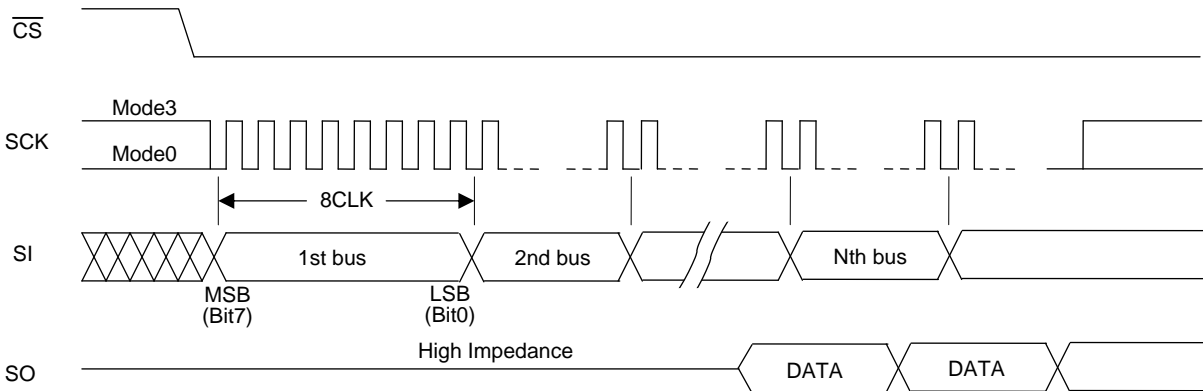


Table 2 Command Settings

Command	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	Nth bus cycle
Read	03h	A23-A16	A15-A8	A7-A0	RD *1	RD *1	RD *1
	0Bh	A23-A16	A15-A8	A7-A0	X	RD *1	RD *1
Small sector erase	20h / D7h	A23-A16	A15-A8	A7-A0			
Sector erase	D8h	A23-A16	A15-A8	A7-A0			
Chip erase	60h / C7h						
Page program	02h	A23-A16	A15-A8	A7-A0	PD *2	PD *2	PD *2
Write enable	06h						
Write disable	04h						
Power down	B9h						
Status register read	05h						
Status register write	01h	DATA					
JEDEC ID read	9Fh						
ID read	ABh	X	X	X			
power down	B9h						
Exit power down mode	ABh						

Explanatory notes for Table 2

"X" signifies "don't care" (that is to say, any value may be input).

The "h" following each code indicates that the number given is in hexadecimal notation.

Addresses A23 to A19 for all commands are "Don't care".

*1: "RD" stands for read data. *2: "PD" stands for page program data.

LE25S40QE

Table 3 Memory Organization

4M Bit

sector(64KB)	small sector	address space(A23 to A0)	
7	127	07F000h	07FFFFh
	to		
6	112	070000h	070FFFh
	to		
5	96	06F000h	06FFFFh
	to		
4	80	060000h	060FFFh
	to		
3	64	05F000h	05FFFFh
	to		
2	48	050000h	050FFFh
	to		
1	32	04F000h	04FFFFh
	to		
0	16	040000h	040FFFh
	to		
	0	03F000h	03FFFFh
	to		
	0	030000h	030FFFh
	to		
	0	02F000h	02FFFFh
	to		
	0	020000h	020FFFh
	to		
	0	01F000h	01FFFFh
	to		
	0	010000h	010FFFh
	to		
	0	00F000h	00FFFFh
	to		
	0	002000h	002FFFh
	to		
	0	001000h	001FFFh
	to		
	0	000000h	000FFFh
	to		

Description of Commands and Their Operations

A detailed description of the functions and operations corresponding to each command is presented below.

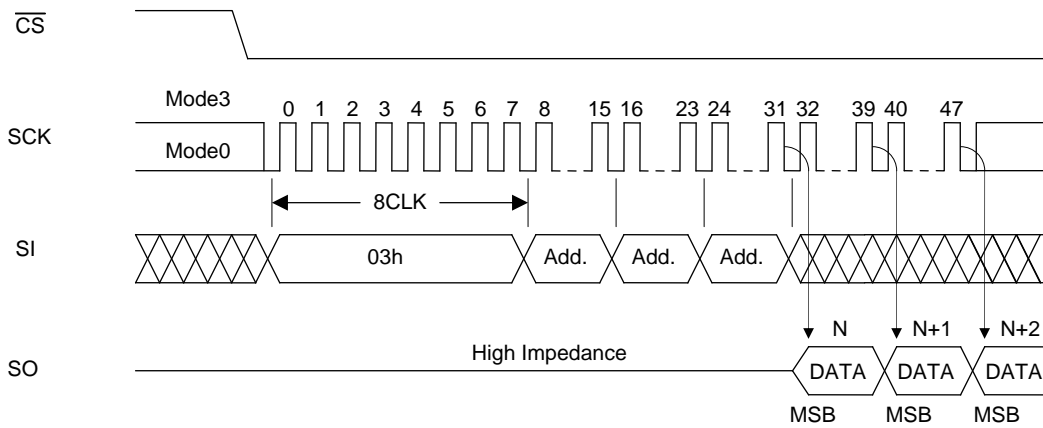
1. Standard SPI read

There are two read commands, the standard SPI read command and High-speed read command.

1-1. Read command

Consisting of the first through fourth bus cycles, the 4 bus cycle read command inputs the 24-bit addresses following (03h). The data is output from SO on the falling clock edge of fourth bus cycle bit 0 as a reference. "Figure 4-a Read" shows the timing waveforms.

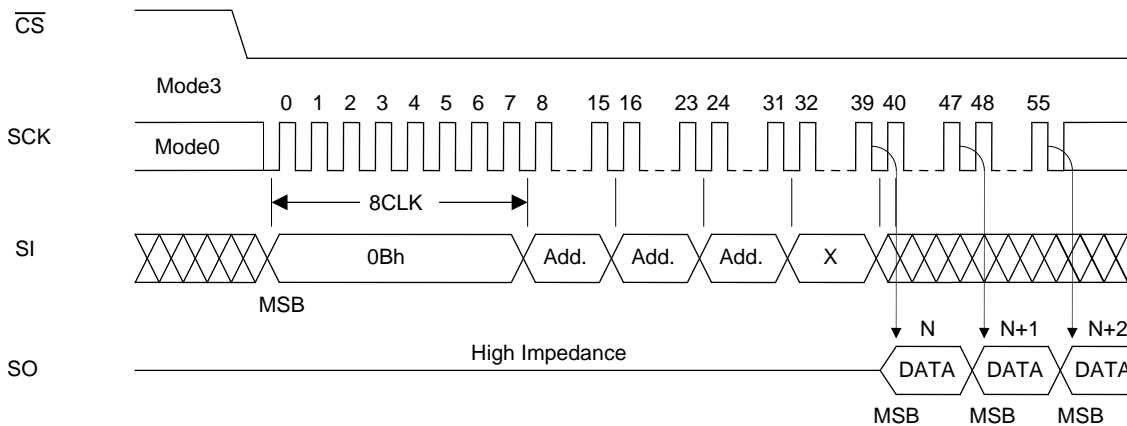
Figure 4-a Read



1-2. High-speed Read command

Consisting of the first through fifth bus cycles, the High-speed read command inputs the 24-bit addresses and 8 dummy bits following (0Bh). The data is output from SO using the falling clock edge of fifth bus cycle bit 0 as a reference. "Figure 4-b High-speed Read" shows the timing waveforms.

Figure 4-b High-speed Read



When SCK is input continuously after the read command has been input and the data in the designated addresses has been output, the address is automatically incremented inside the device while SCK is being input, and the corresponding data is output in sequence. If the SCK input is continued after the internal address arrives at the highest address (7FFFh), the internal address returns to the lowest address (0000h), and data output is continued. By setting the logic level of \overline{CS} to high, the device is deselected, and the read cycle ends. While the device is deselected, the output pin SO is in a high-impedance state.

2. Status Registers

The status registers hold the operating and setting statuses inside the device, and this information can be read (status register read) and the protect information can be rewritten (status register write). There are 8 bits in total, and "Table 4 Status registers" gives the significance of each bit.

Table 4 Status Registers

Bit	Name	Logic	Function	Power-on Time Information
Bit0	$\overline{\text{RDY}}$	0	Ready	0
		1	Erase/Program	
Bit1	WEN	0	Write disabled	0
		1	Write enabled	
Bit2	BP0	0	Block protect information Protecting area switch	Nonvolatile information
		1		
Bit3	BP1	0		
		1		
Bit4	BP2	0		Nonvolatile information
		1		
Bit5	TB	0	Block protect Upper side/Lower side switch	Nonvolatile information
		1		
Bit6			Reserved bits	0
Bit7	SRWP	0	Status register write enabled	Nonvolatile information
		1	Status register write disabled	

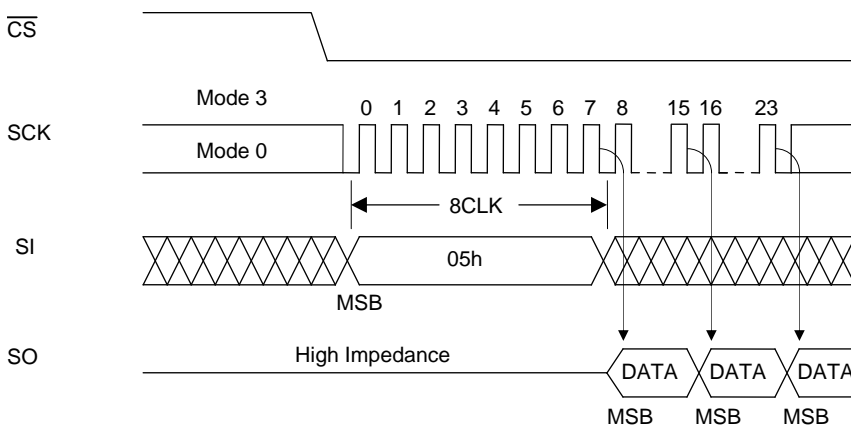
2-1. Status register read

The contents of the status registers can be read using the status register read command. This command can be executed even during the following operations.

- Small sector erase, sector erase, chip erase
- Page program
- Status register write

"Figure 5 Status Register Read" shows the timing waveforms of status register read. Consisting only of the first bus cycle, the status register command outputs the contents of the status registers synchronized to the falling edge of the clock (SCK) with which the eighth bit of (05h) has been input. In terms of the output sequence, SRWP (bit 7) is the first to be output, and each time one clock is input, all the other bits up to $\overline{\text{RDY}}$ (bit 0) are output in sequence, synchronized to the falling clock edge. If the clock input is continued after $\overline{\text{RDY}}$ (bit 0) has been output, the data is output by returning to the bit (SRWP) that was first output, after which the output is repeated for as long as the clock input is continued. The data can be read by the status register read command at any time (even during a program or erase cycle).

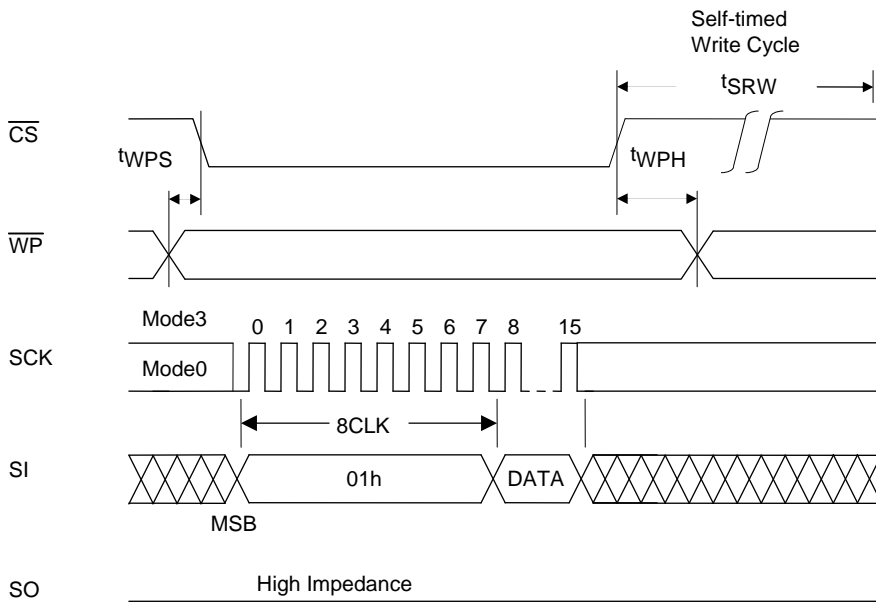
Figure 5 Status Register Read



2-2. Status register write

The information in status registers BP0, BP1, BP2, TB and SRWP can be rewritten using the status register write command. RDY, WEN and bit 6 are read-only bits and cannot be rewritten. The information in bits BP0, BP1, BP2, TB and SRWP is stored in the non-volatile memory, and when it is written in these bits, the contents are retained even at power-down. "Figure 6 Status Register Write" shows the timing waveforms of status register write, and Figure 19 shows a status register write flowchart. Consisting of the first and second bus cycles, the status register write command initiates the internal write operation at the rising \overline{CS} edge after the data has been input following (01h). Erase and program are performed automatically inside the device by status register write so that erasing or other processing is unnecessary before executing the command. By the operation of this command, the information in bits BP0, BP1, BP2, TB and SRWP can be rewritten. Since bits RDY (bit 0), WEN (bit 1) and bit 6 of the status register cannot be written, no problem will arise if an attempt is made to set them to any value when rewriting the status register. Status register write ends can be detected by RDY of status register read. To initiate status register write, the logic level of the WP pin must be set high and status register WEN must be set to "1".

Figure 6 Status Register Write



2-3. Contents of each status register

RDY (Bit 0)

The RDY register is for detecting the write (program, erase and status register write) end. When it is "1", the device is in a busy state, and when it is "0", it means that write is completed.

WEN (bit 1)

The WEN register is for detecting whether the device can perform write operations. If it is set to "0", the device will not perform the write operation even if the write command is input. If it is set to "1", the device can perform write operations in any area that is not block-protected.

WEN can be controlled using the write enable and write disable commands. By inputting the write enable command (06h), WEN can be set to "1"; by inputting the write disable command (04h), it can be set to "0." In the following states, WEN is automatically set to "0" in order to protect against unintentional writing.

- At power-on
- Upon completion of small sector erase, sector erase or chip erase
- Upon completion of page program
- Upon completion of status register write

* If a write operation has not been performed inside the LE25S40QE because, for instance, the command input for any of the write operations (small sector erase, sector erase, chip erase, page program, or status register write) has failed or a write operation has been performed for a protected address, WEN will retain the status established prior to the issue of the command concerned. Furthermore, its state will not be changed by a read operation.

BP0, BP1, BP2, TB (Bits 2, 3, 4, 5)

Block protect BP0, BP1, BP2 and TB are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to "Table 5 Protect level setting conditions".

BP0, BP1, and BP2 are used to select the protected area and TB to allocate the protected area to the higher-order address area or lower-order address area.

Table 5 Protect Level Setting Conditions

Protect Level	Status Register Bits				Protected Area
	TB	BP2	BP1	BP0	
0 (Whole area unprotected)	X	0	0	0	None
T1 (Upper side 1/8 protected)	0	0	0	1	07FFFFh to 070000h
T2 (Upper side 1/4 protected)	0	0	1	0	07FFFFh to 060000h
T3 (Upper side 1/2 protected)	0	0	1	1	07FFFFh to 040000h
B1 (Lower side 1/8 protected)	1	1	0	1	00FFFFh to 000000h
B2 (Lower side 1/4 protected)	1	1	1	0	01FFFFh to 000000h
B3 (Lower side 1/2 protected)	1	1	1	1	03FFFFh to 000000h
4 (Whole area protected)	X	1	X	X	07FFFFh to 000000h

* Chip erase is enabled only when the protect level is 0.

SRWP (bit 7)

Status register write protect SRWP is the bit for protecting the status registers, and its information can be rewritten. When SRWP is "1" and the logic level of the \overline{WP} pin is low, the status register write command is ignored, and status registers BP0, BP1, BP2, TB and SRWP are protected. When the logic level of the \overline{WP} pin is high, the status registers are not protected regardless of the SRWP state. The SRWP setting conditions are shown in "Table 6 SRWP setting conditions".

Table 6 SRWP Setting Conditions

\overline{WP} Pin	SRWP	Status Register Protect State
0	0	Unprotected
	1	Protected
1	0	Unprotected
	1	Unprotected

Bit 6 are reserved bits, and have no significance.

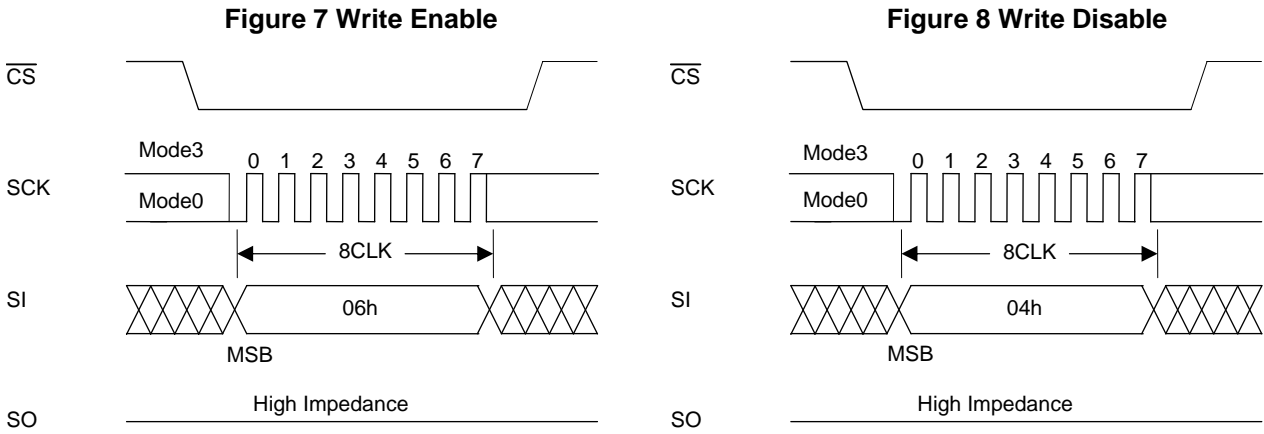
3. Write Enable

Before performing any of the operations listed below, the device must be placed in the write enable state. Operation is the same as for setting status register WEN to "1", and the state is enabled by inputting the write enable command. "Figure 7 Write Enable" shows the timing waveforms when the write enable operation is performed. The write enable command consists only of the first bus cycle, and it is initiated by inputting (06h).

- Small sector erase, sector erase, chip erase
- Page program
- Status register write

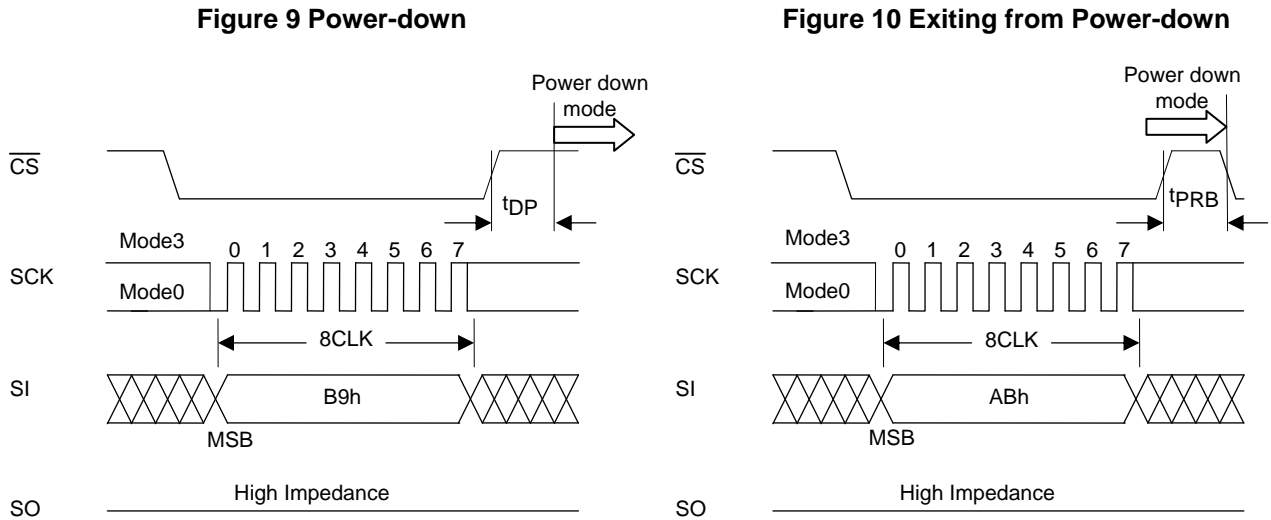
4. Write Disable

The write disable command sets status register WEN to "0" to prohibit unintentional writing. "Figure 8 Write Disable" shows the timing waveforms. The write disable command consists only of the first bus cycle, and it is initiated by inputting (04h). The write disable state (WEN "0") is exited by setting WEN to "1" using the write enable command (06h).



5. Power-down

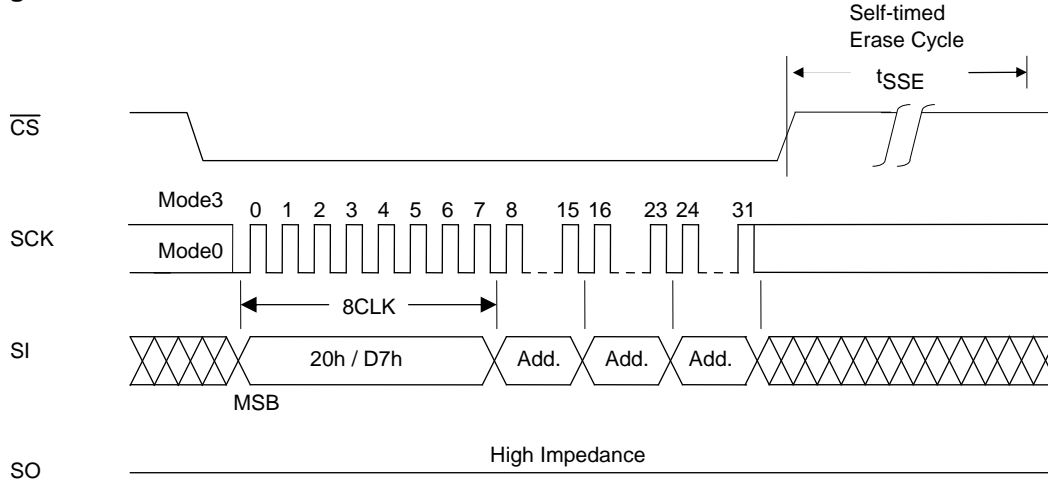
The power-down command sets all the commands, with the exception of the silicon ID read command and the command to exit from power-down, to the acceptance prohibited state (power-down). "Figure 9 Power-down" shows the timing waveforms. The power-down command consists only of the first bus cycle, and it is initiated by inputting (B9h). However, a power-down command issued during an internal write operation will be ignored. The power-down state is exited using the power-down exit command (power-down is exited also when one bus cycle or more of the silicon ID read command (ABh) has been input). "Figure 10 Exiting from Power-down" shows the timing waveforms of the power-down exit command.



6. Small Sector Erase

Small sector erase is an operation that sets the memory cell data in any small sector to "1". A small sector consists of 4Kbytes. "Figure 11 Small Sector Erase" shows the timing waveforms, and Figure 20 shows a small sector erase flowchart. The small sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (20h) or (D7h). Addresses A18 to A12 are valid, and Addresses A23 to A19 are "don't care". After the command has been input, the internal erase operation starts from the rising \overline{CS} edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register RDY.

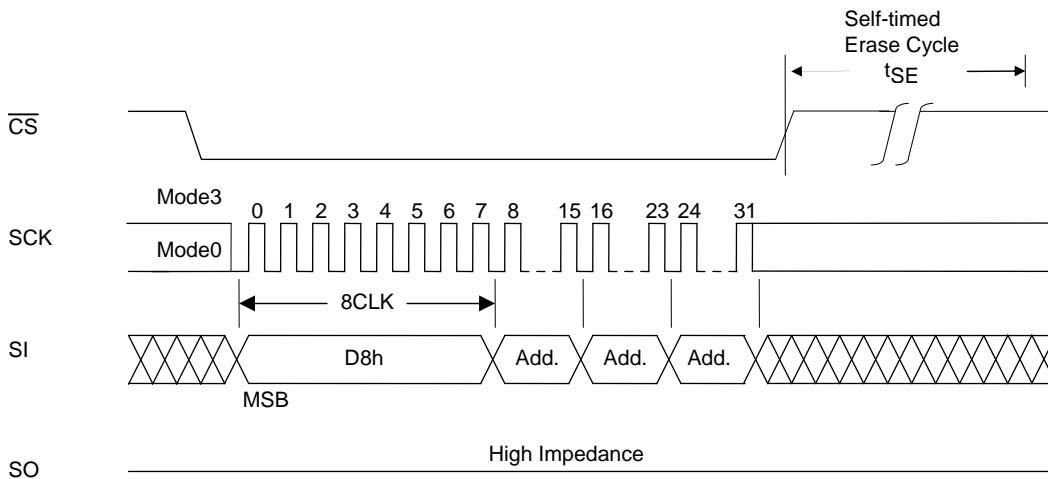
Figure 11 Small Sector Erase



7. Sector Erase

Sector erase is an operation that sets the memory cell data in any sector to "1". A sector consists of 64Kbytes. "Figure 12 Sector Erase" shows the timing waveforms, and Figure 20 shows a sector erase flowchart. The sector erase command consists of the first through fourth bus cycles, and it is initiated by inputting the 24-bit addresses following (D8h). Addresses A18 to A16 are valid, and Addresses A23 to A19 are "don't care". After the command has been input, the internal erase operation starts from the rising \overline{CS} edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register RDY.

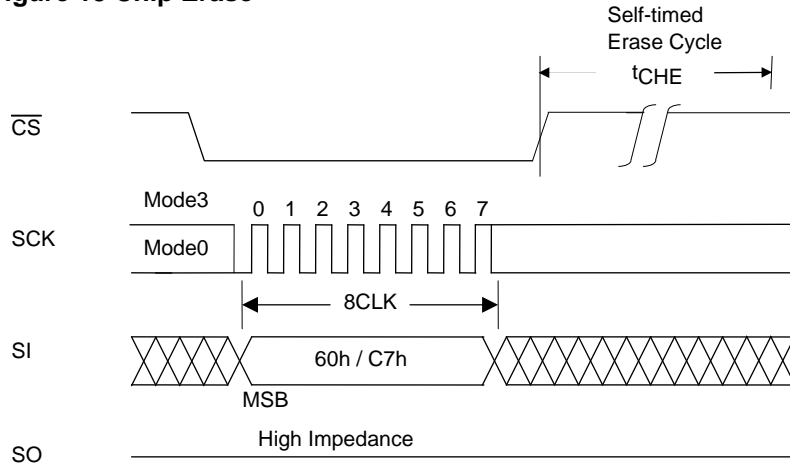
Figure 12 Sector Erase



8. Chip Erase

Chip erase is an operation that sets the memory cell data in all the sectors to "1". "Figure 13 Chip Erase" shows the timing waveforms, and Figure 20 shows a chip erase flowchart. The chip erase command consists only of the first bus cycle, and it is initiated by inputting (60h) or (C7h). After the command has been input, the internal erase operation starts from the rising \overline{CS} edge, and it ends automatically by the control exercised by the internal timer. Erase end can also be detected using status register \overline{RDY} .

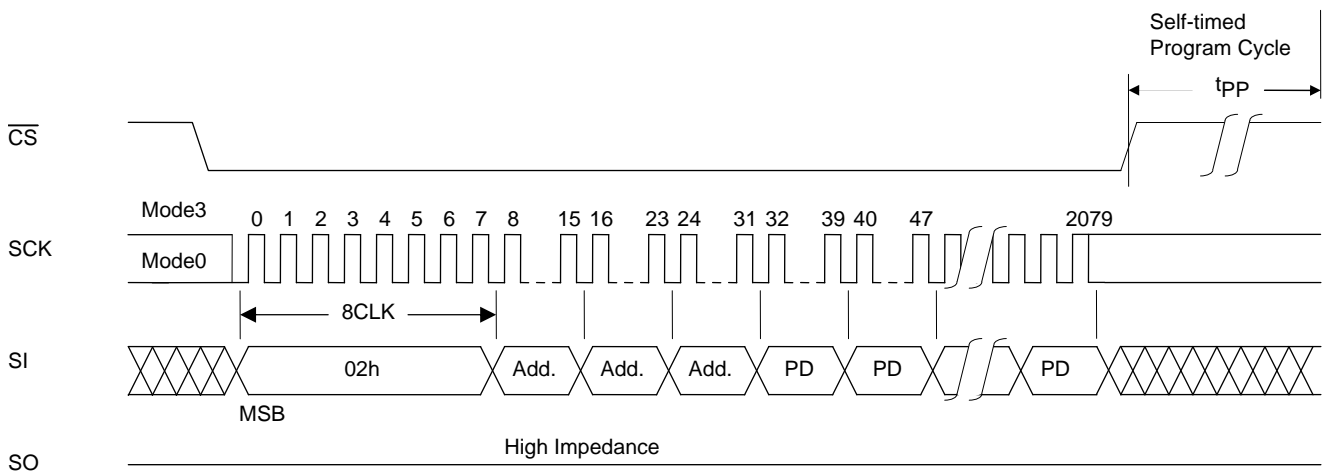
Figure 13 Chip Erase



9. Page Program

Page program is an operation that programs any number of bytes from 1 to 256 bytes within the same sector page (page addresses: A18 to A8). Before initiating page program, the data on the page concerned must be erased using small sector erase, sector erase, or chip erase. "Figure 14 Page Program" shows the page program timing waveforms, and Figure 21 shows a page program flowchart. After the falling \overline{CS} edge, the command (02H) is input followed by the 24-bit addresses. Addresses A18 to A0 are valid. The program data is then loaded at each rising clock edge until the rising \overline{CS} edge, and data loading is continued until the rising \overline{CS} edge. If the data loaded has exceeded 256 bytes, the 256 bytes loaded last are programmed. The program data must be loaded in 1-byte increments, and the program operation is not performed at the rising \overline{CS} edge occurring at any other timing.

Figure 14 Page Program



10. Silicon ID Read

ID read is an operation that reads the manufacturer code and device ID information. The silicon ID read command is not accepted during writing. There are two methods of reading the silicon ID, each of which is assigned a device ID. In the first method, the read command sequence consists only of the first bus cycle in which (9Fh) is input. In the subsequent bus cycles, the manufacturer code 62h which is assigned by JEDEC, 2-byte device ID code (memory type, memory capacity), and reserved code are output sequentially. The 4-byte code is output repeatedly as long as clock inputs are present, "Table 7-1 JEDEC ID code " lists the silicon ID codes and "Figure 15-a JEDEC ID read" shows the JEDEC ID read timing waveforms.

The second method involves inputting the ID read command. This command consists of the first through fourth bus cycles, and the one bite silicon ID can be read when 24 dummy bits are input after (ABh). "Table 7-2 ID code " lists the silicon ID codes and "Figure 15-b ID read" shows the ID read timing waveforms.

If the SCK input persists after a device code is read, that device code continues to be output. The data output is transmitted starting at the falling edge of the clock for bit 0 in the fourth bus cycle and the silicon ID read sequence is finished by setting CS high.

Table 7-1 JEDEC ID code

		Output code
Manufacturer code		62h
2 byte device ID	Memory type	16h
	Memory capacity code	13h(4M Bit)
Device code	1	00h

Table 7-2 ID code

	Output Code
1 byte device ID	3E (LE25S40QE)

Figure 15-a JEDEC ID Read

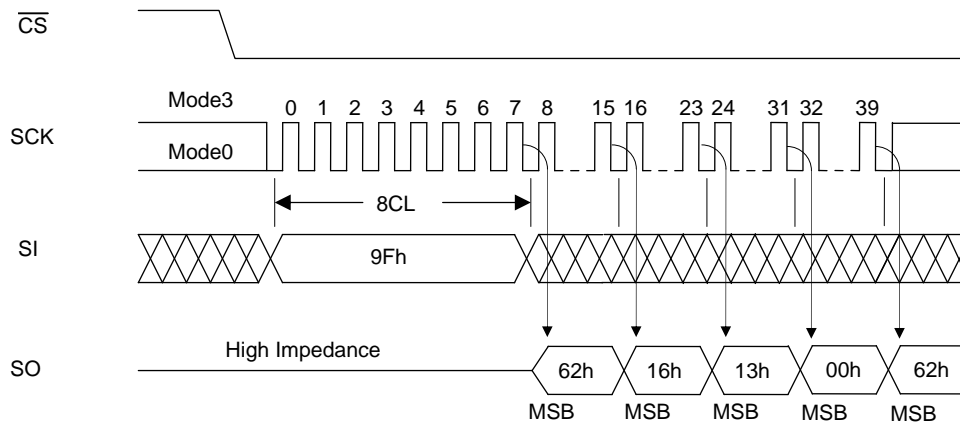
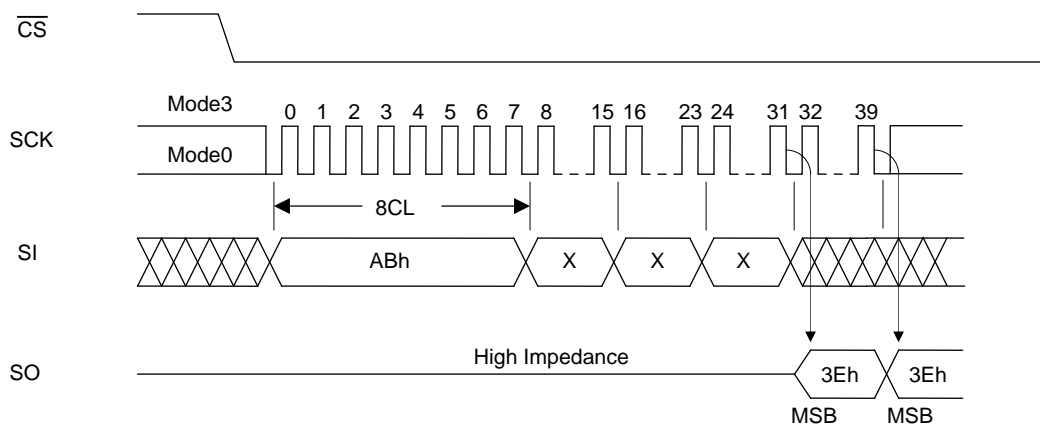


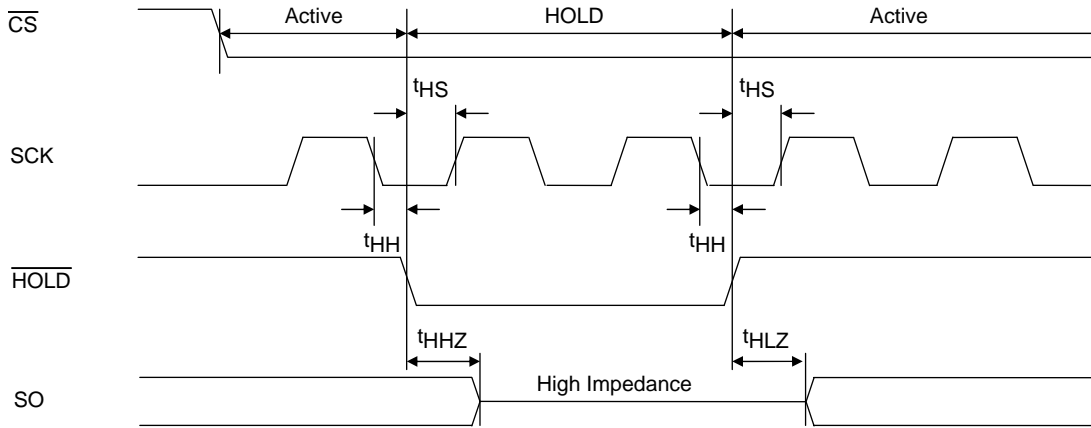
Figure 15-b ID Read



11. Hold Function

Using the $\overline{\text{HOLD}}$ pin, the hold function suspends serial communication (it places it in the hold status). "Figure16 $\overline{\text{HOLD}}$ " shows the timing waveforms. The device is placed in the hold status at the falling $\overline{\text{HOLD}}$ edge while the logic level of SCK is low, and it exits from the hold status at the rising $\overline{\text{HOLD}}$ edge. When the logic level of SCK is high, $\overline{\text{HOLD}}$ must not rise or fall. The hold function takes effect when the logic level of $\overline{\text{CS}}$ is low, the hold status is exited and serial communication is reset at the rising $\overline{\text{CS}}$ edge. In the hold status, the SO output is in the high-impedance state, and SI and SCK are "don't care".

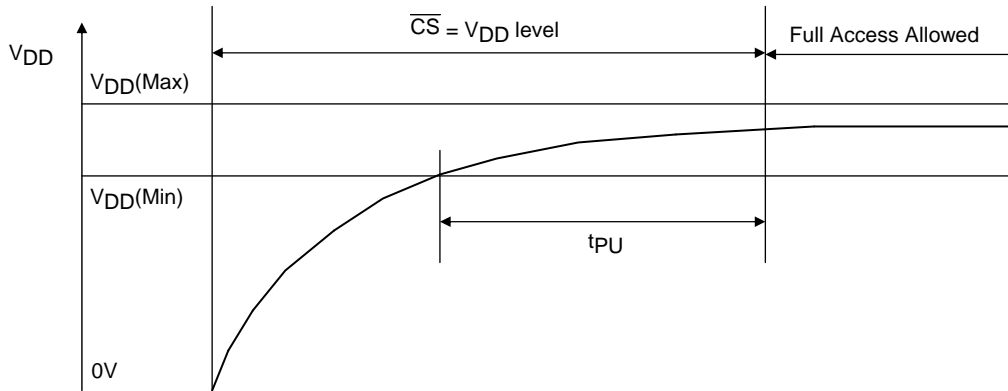
Figure 16 $\overline{\text{HOLD}}$



12. Power-on

In order to protect against unintentional writing, $\overline{\text{CS}}$ must be within at $V_{\text{DD}}-0.3$ to $V_{\text{DD}}+0.3$ on power-on. After power-on, the supply voltage has stabilized at V_{DD} min. or higher, waits for t_{PU} before inputting the command to start a device operation. The device is in the standby state and not in the power-down state after power is turned on. To put the device into the power-down state, it is necessary to enter a power-down command.

Figure 17 Power-on Timing

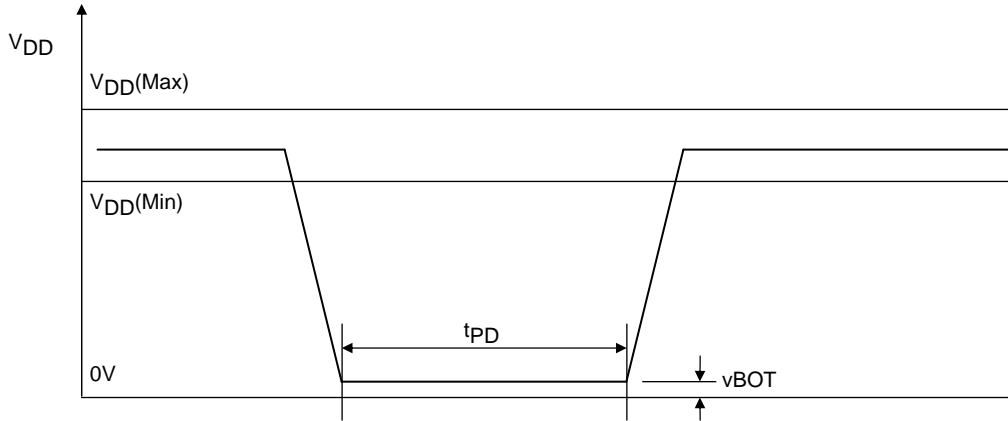


13. Hardware Data Protection

LE25S40QE incorporates a power-on reset function. The following conditions must be met in order to ensure that the power reset circuit will operate stably.

No guarantees are given for data in the event of an instantaneous power failure occurring during the writing period.

Figure 18 Power-down Timing



Power-on timing

Parameter	Symbol	spec		unit
		min	max	
power-on to operation time	t _{PU}	100		μs
power-down time	t _{PD}	10		ms
power-down voltage	t _{BOT}		0.2	V

14. Software Data Protection

The LE25S40QE eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

- When a write command is input and the rising \overline{CS} edge timing is not in a bus cycle (8 CLK units of SCK)
- When the page program data is not in 1-byte increments
- When the status register write command is input for 2 bus cycles or more

15. Decoupling Capacitor

A 0.1μF ceramic capacitor must be provided to each device and connected between VDD and VSS in order to ensure that the device will operate stably.

LE25S40QE

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage	VDDmax	With respect to VSS	-0.5 to +2.4	V
DC voltage (all pins)	VIN/VOUT	With respect to VSS	-0.5 to VDD+0.5	V
Storage temperature	Tstg		-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Operating Conditions

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage	VDD		1.65 to 1.95	V
Operating ambient temperature	Topr		-40 to +85	°C

Allowable DC Operating Conditions

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Read mode operating current	ICCR	SCK=0.1VDD/0.9VDD, HOLD=WP=0.9VDD, SO=open,25MHz			6	mA
		SCK=0.1VDD/0.9VDD, HOLD=WP=0.9VDD, SO=open,40MHz			8	mA
Write mode operating current (erase+page program)	ICCW	tSSE= tSE= tCHE=typ..tpp=max			15	mA
CMOS standby current	ISB	CS=VDD, HOLD=WP=VDD, SI=VSS/VDD, SO=open,			50	µA
Power-down standby current	IDSB	CS=VDD, HOLD=WP=VDD, SI=VSS/VDD, SO=open,			10	µA
Input leakage current	ILI				2	µA
Output leakage current	ILO				2	µA
Input low voltage	VIL		-0.3		0.3VDD	V
Input high voltage	VIH		0.7VDD		VDD+0.3	V
Output low voltage	VOL	IOL=100µA, VDD=VDD min			0.2	V
		IOL=1.6mA, VDD=VDD min			0.4	
Output high voltage	VOH	IOH=-100µA, VDD=VDD min	VCC-0.2			V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Data hold, Rewriting frequency

Parameter	condition	min	max	unit
Rewriting frequency	Program/Erase	100,000		times/ Sector
	Status resistor write	1,000		
Data hold		20		year

Pin Capacitance at Ta=25°C, f=1MHz

Parameter	Symbol	Conditions	Ratings	unit
			max	
Output pin capacitance	C _{SO}	V _{SO} =0V	12	pF
Input pin Capacitance	C _{IN}	V _{IN} =0V	6	pF

Note: These parameter values do not represent the results of measurements undertaken for all devices but rather values for some of the sampled devices.

LE25S40QE

AC Characteristics

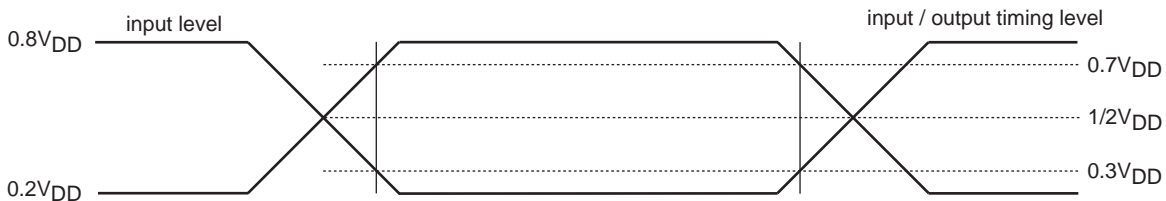
Parameter		Symbol	Ratings			unit
			min	typ	max	
Clock frequency	Read instruction(03h)	f _{CLK}			25	MHz
	All instructions except for read(03h)				40	MHz
Input signal rising/falling time		t _{RF}	0.1			V/ns
SCK logic high level pulse width	25MHz	t _{CLHI}	14			ns
	40MHz		11.5			
SCK logic low level pulse width	25MHz	t _{CLLO}	14			ns
	40MHz		11.5			
$\overline{\text{CS}}$ setup time		t _{CSS}	10			ns
$\overline{\text{CS}}$ hold time		t _{CSH}	10			ns
Data setup time		t _{DS}	5			ns
Data hold time		t _{DH}	5			ns
$\overline{\text{CS}}$ wait pulse width		t _{CPH}	25			ns
Output high impedance time from $\overline{\text{CS}}$		t _{CHZ}			15	ns
Output data time from SCK		t _v		8	11	ns
Output data hold time		t _{HO}	1			ns
Output low impedance time from SCK		t _{CLZ}	0			ns
$\overline{\text{WP}}$ setup time		t _{WPS}	20			ns
$\overline{\text{WP}}$ hold time		t _{WPH}	20			ns
$\overline{\text{HOLD}}$ setup time		t _{HS}	5			ns
$\overline{\text{HOLD}}$ hold time		t _{HH}	5			ns
Output low impedance time from $\overline{\text{HOLD}}$		t _{HLZ}			12	ns
Output high impedance time from $\overline{\text{HOLD}}$		t _{HHZ}			9	ns
Power-down time		t _{DP}			5	μs
Power-down recovery time		t _{PRB}			5	μs
Write status register time		t _{SRW}		8	10	ms
Page programming cycle time	256Byte	t _{PP}		6	8	ms
	nByte			0.15+ n*5.85/256	0.20+ n*7.80/256	ms
Small sector erase cycle time		t _{SSE}		0.04	0.15	s
Sector erase cycle time		t _{SE}		0.08	0.25	s
Chip erase cycle time		t _{CHE}		0.3	3.0	s

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC Test Conditions

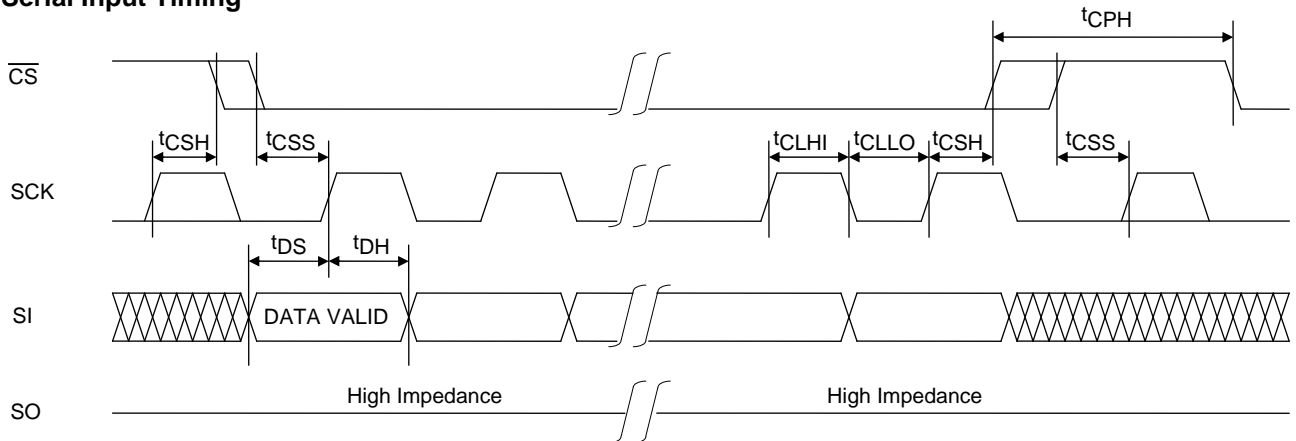
- Input pulse level 0.2V_{DD} to 0.8V_{DD}
- Input rising/falling time .. 5ns
- Input timing level 0.3V_{DD}, 0.7V_{DD}
- Output timing level 1/2×V_{DD}
- Output load 15pF

Note: As the test conditions for "typ", the measurements are conducted using 1.8V for V_{DD} at room temperature.

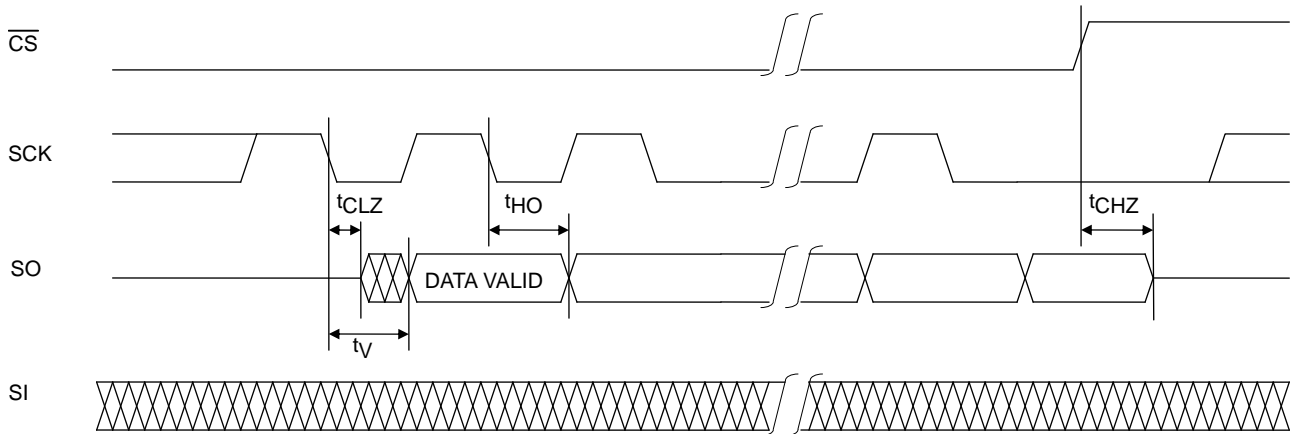


Timing waveforms

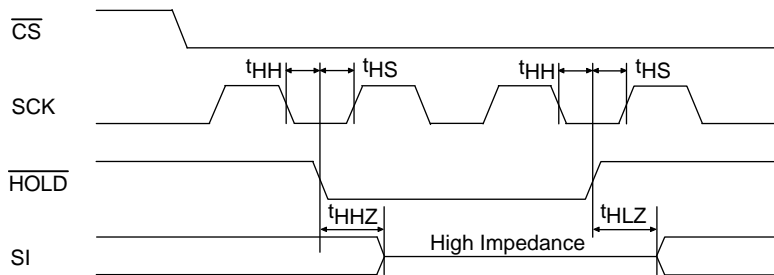
Serial Input Timing



Serial Output Timing



Hold Timing



Status register write Timing

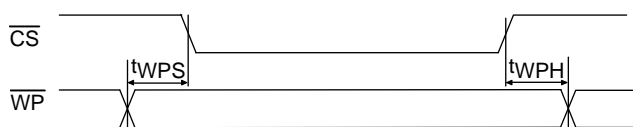
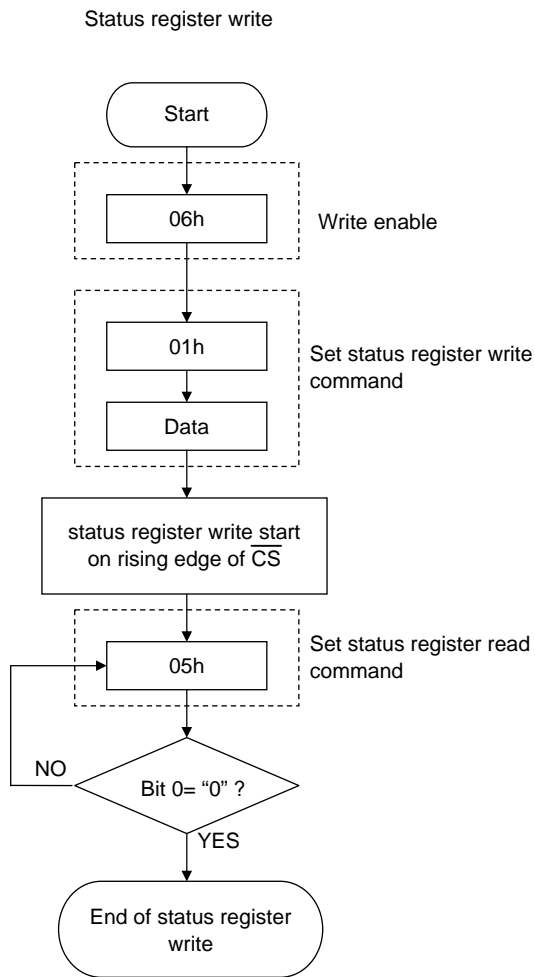


Figure 19 Status Register Write Flowchart



* Automatically placed in write disabled state at the end of the status register write

Figure 20 Erase Flowcharts

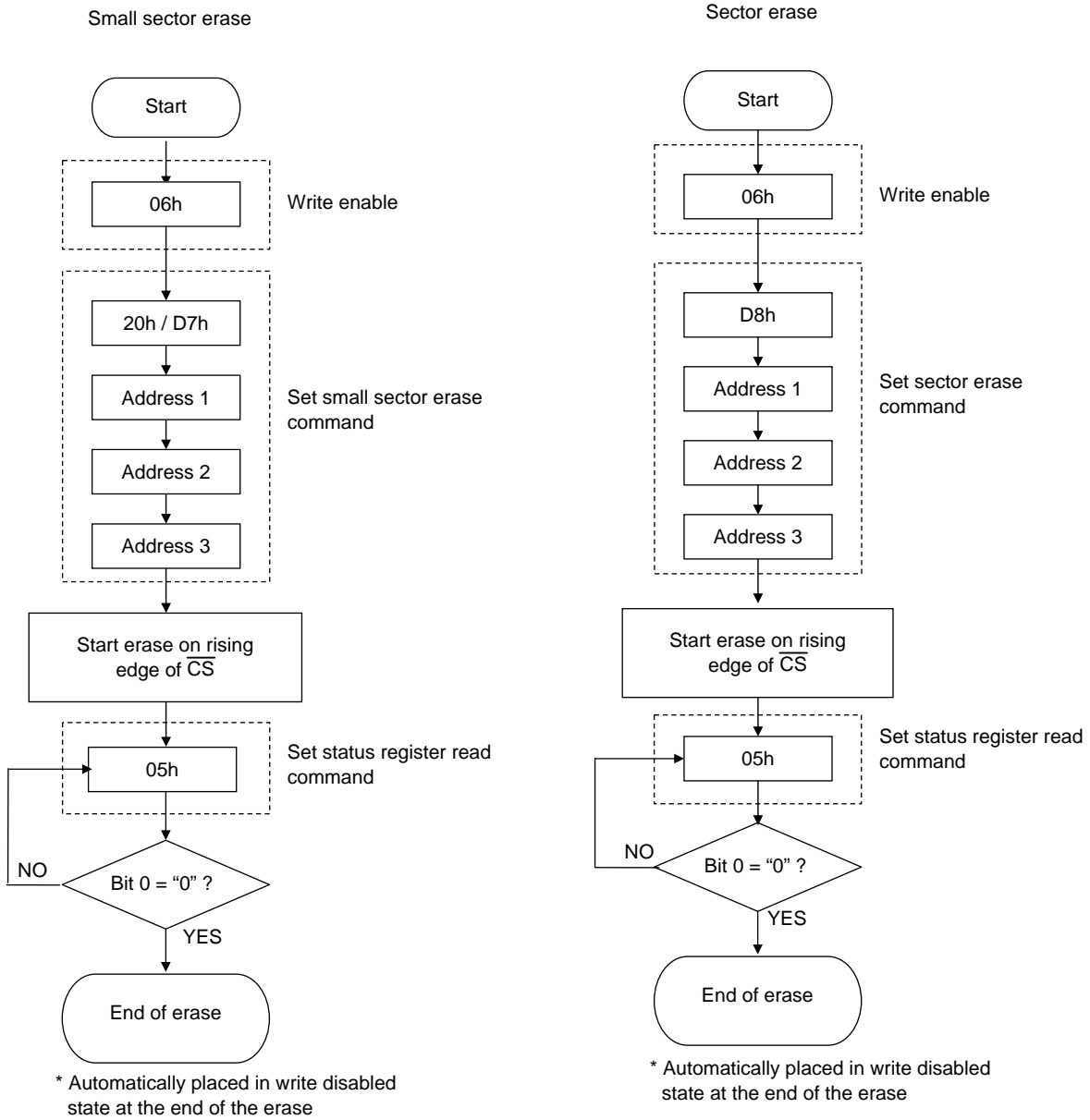
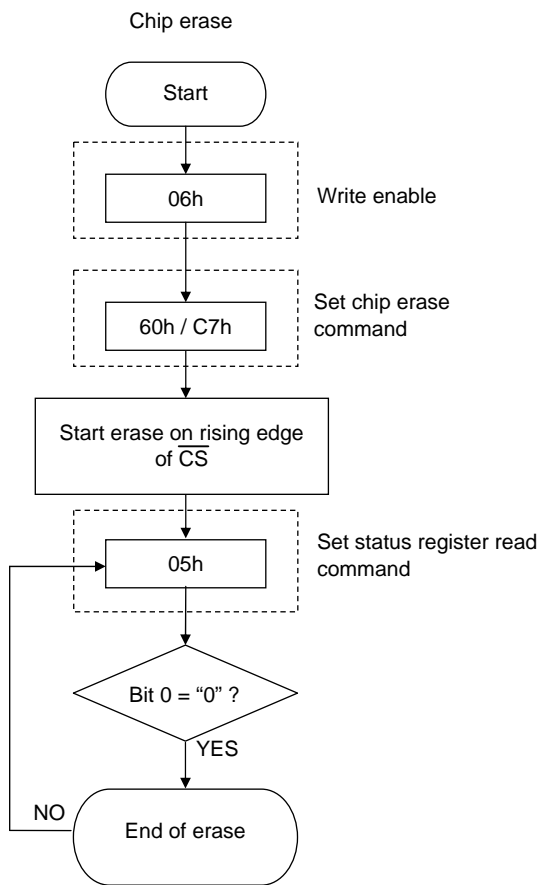
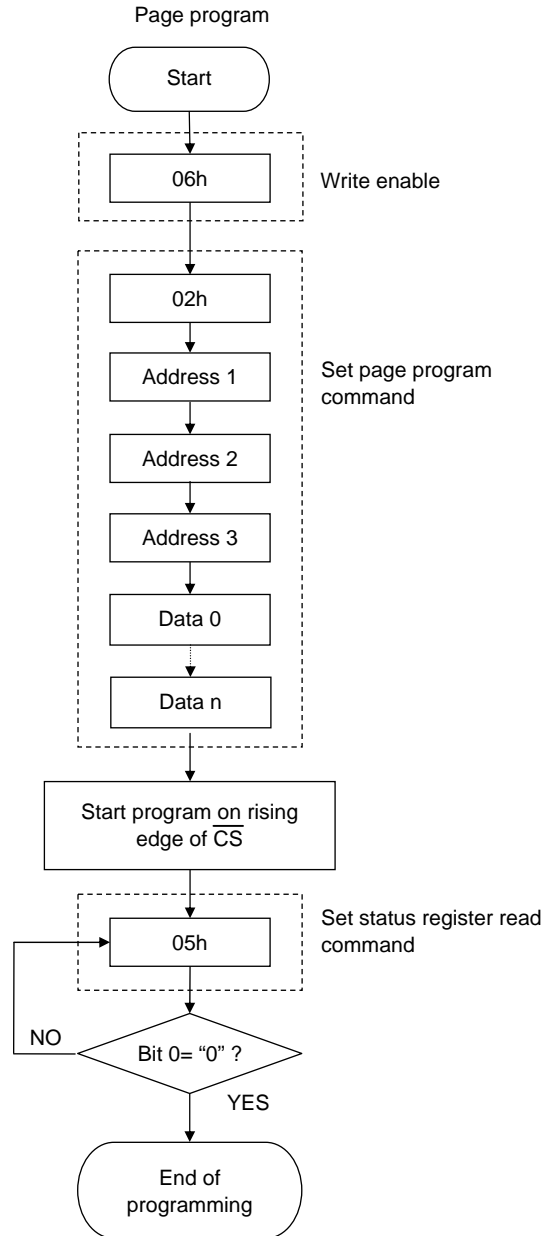


Figure 21 Page Program Flowchart



* Automatically placed in write disabled state at the end of the erase



* Automatically placed in write disabled state at the end of the programming operation.

LE25S40QE

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LE25S40QE-AH	VDFN8 5x6 (Pb-Free / Halogen Free)	2000 / Tape & Reel

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